TCAE32 - Force & Capacitive Touch Sensing Controller

1. Features

- 32-bit Low Power Arm® Cortex®-M0 CPU core
- Memory
  - 64KB Flash
  - 8KB SRAM
- Clocks
  - On-chip 16-MHz RC oscillator
  - On-chip 32-MHz clock with frequency doubler
  - On-chip 32-KHz RC oscillator
- 16-bit RTC
  - Up to 4 different timeout thresholds
  - Periodical timeout events once enabled
- UART
  - Full duplex series communication
  - Support LIN Slave function
- Print UART, Transmission only for debug
- I2C
  - Standard speed（100KHz）and fast speed（400KHz）
  - Master and slave mode
- SPI
  - Master and slave mode
- DMA
  - 8 channels for I2C/UART0/SPI/ADC/TinyTouch
- GPT0/1/2/3/4
  - 16-bit general purpose timer/counter
  - Multiple modes supporting PWM generation
- TinyTouch
  - Integrates two touch blocks with run in parallel
  - With external reference capacitor
  - 26 channels for 48-pin package and 19 channels for 32-pin package
  - Comparator based or ADC based detection
  - Configurable frequency hopping
- ADC
  - 14-bit SAR ADC
  - Sampling rate up to 1MSPS
  - 8 differential or 16 single-end external channels
  - 2-stage PGA, up to 1024x gain
  - Offset voltage cancellation
- LDOVS
  - 8-level adjustable voltages from 1.8V to 3.1V
  - 15mA minimum
- On-chip temperature sensor
- GPIO
  - Up to 45 GPIOs for QFN48 package
  - Up to 29 GPIOs for QFN32 package
- UUID, 96-bit unique identifier
- Low- power modes
  - IDLE mode
  - SLEEPWALK mode
  - SLEEP mode
- Tinywork® mechanism
- POR
- LVD
- Watchdog WDG
- 2-pin Serial Wire Debug Interface (SWD)
- AEC-Q100 Grade2 Qualified
- Operating voltage range: 2.8V~5.5V
- Package：QFN32, QFN48
- ESD: 8KV (HBM)

2. Applications

- Automotive intelligent interior and smart surface
- Automotive force and cap-touch sensing for HMI applications, i.e., central console buttons, reading lamp buttons, door touch detection, steering wheel hands off detection (HOD), etc.

3. Description

TCAE32 is an AEC-Q100 qualified low-power CMOS 32-bit Arm® Cortex®-M0 MCU, designed for force sensing and capacitive touch. It supports 8-channel force sensing detection, and up-to-26 channel capacitive touch detection.

The MCU integrates Wheatstone bridge AFE circuits, including low noise LDO (LDOVS), two-stage PGA with up to 1024x gain, 14-bit high resolution ADC, and offset canceling circuit. The PGA can cancel offset voltage while amplify weak signal variance (i.e. <10uV) which is interested, before the signal enters the ADC. The device also integrates TinyTouch module to implement self-capacitance touch sensing with detection algorithm.

Part Number	Package	Body Size (Nom.)
TCAE32A-QKA2	QFN48	7mm × 7mm
TCAE32A-QFA2	QFN32	5mm × 5mm

Carrier type: Tape & Reel, with 3000 pieces per reel.

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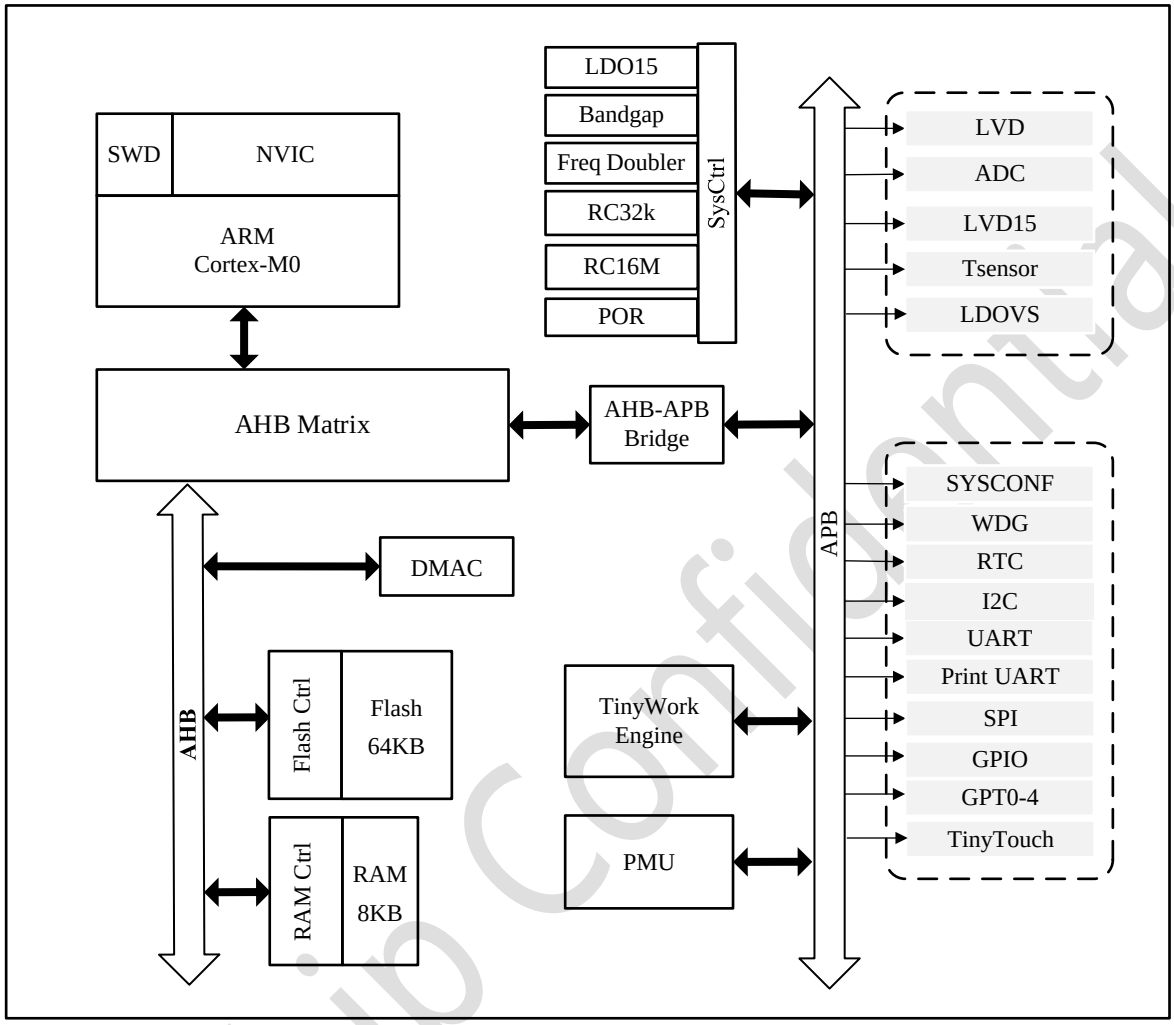
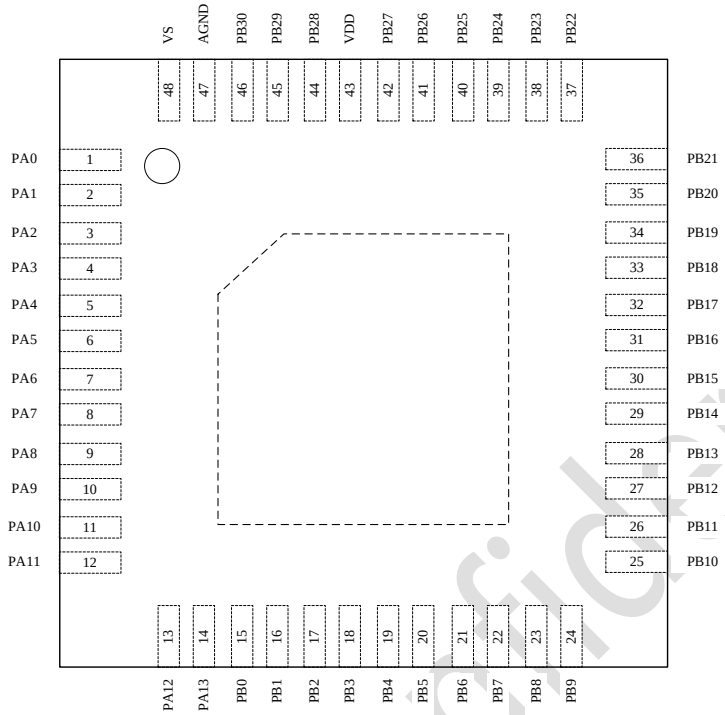
4. Block Diagram



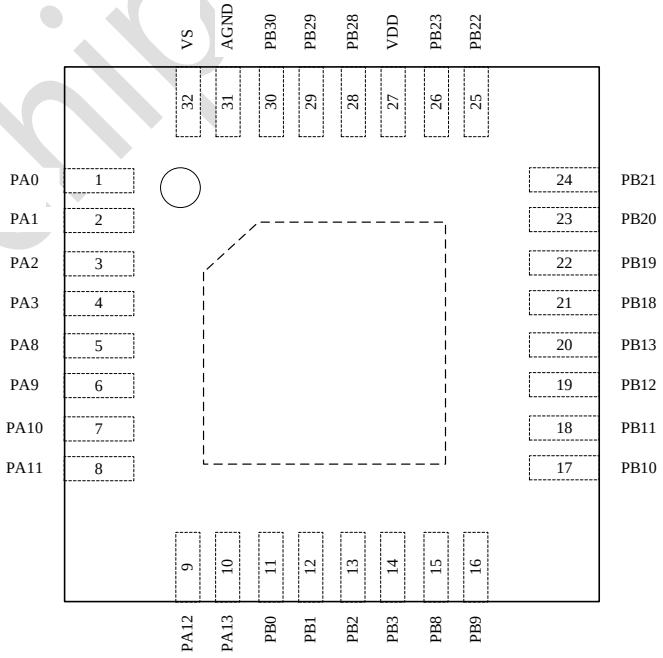
5. Pinout

5.1. 48-Pin QFN



48-Pin QFN Top View

5.2. 32-Pin QFN



32-Pin QFN Top View

5.3. PIN Functions

PIN Number QFN48	PIN Number QFN32	PIN Name	Property	Description
43	27	VDD	P	Power supply pin
47	31	AGND	P	Ground
48	32	VS	P	LDO output, to power the external sensors. Connect a 22nF capacitor to ground.
1	1	PA0	AIO/DIO	PA0: GPIO TCP0: Cap touch channel 0 positive terminal AIP0: ADC input channel 0 positive terminal
2	2	PA1	AIO/DIO	PA1: GPIO TCN0: Cap touch channel 0 negative terminal AIN0: ADC input channel 0 negative terminal
3	3	PA2	AIO/DIO	PA2: GPIO TCP1: Cap touch channel 1 positive terminal AIP1: ADC input channel 1 positive terminal
4	4	PA3	AIO/DIO	PA3: GPIO TCN1: Cap touch channel 1 negative terminal AIN1: ADC input channel 1 negative terminal
5	-	PA4	AIO/DIO	PA4: GPIO TCP2: Cap touch channel 2positive terminal AIP2: ADC input channel 2 positive terminal
6	-	PA5	AIO/DIO	PA5: GPIO TCN2: Cap touch channel 2negative terminal AIN2: ADC input channel 2negative terminal
7	-	PA6	AIO/DIO	PA6: GPIO TCP3: Cap touch channel 3 positive terminal AIP3: ADC input channel 3 positive terminal
8	-	PA7	AIO/DIO	PA7: GPIO TCN3: Cap touch channel 3 negative terminal AIN3: ADC input channel 3 negative terminal
9	5	PA8	AIO/DIO	PA8: GPIO TCP4: Cap touch channel 4 positive terminal

				AIP4: ADC input channel 4 positive terminal CREF0: reference capacitor for Touch Block0
10	6	PA9	AIO/DIO	PA9: GPIO TCN4: Cap touch channel 4 negative terminal AIN4: ADC input channel 4 negative terminal
11	7	PA10	AIO/DIO	PA10: GPIO TCP5: Cap touch channel 5 positive terminal AIP5: ADC input channel 5 positive terminal
12	8	PA11	AIO/DIO	PA11: GPIO TCN5: Cap touch channel 5 negative terminal AIN5: ADC input channel 5 negative terminal
13	9	PA12	AIO/DIO	PA12: GPIO TCP6: Cap touch channel 6 positive terminal AIP6: ADC input channel 6 positive terminal
14	10	PA13	AIO/DIO	PA13: GPIO TCN6: Cap touch channel 6 negative terminal AIN6: ADC input channel 6 negative terminal
15	11	PB0	AIO/DIO	PB0: GPIO TCP7: Cap touch channel 7 positive terminal AIP7: ADC input channel 7 positive terminal CREF1: reference capacitor for Touch Block1 PRINT_UART_TX: Print UART TX pin
16	12	PB1	AIO/DIO	PB1: GPIO TCN7: Cap touch channel 7 negative terminal AIN7: ADC input channel 7 negative terminal
17	13	PB2	AIO/DIO	PB2: GPIO TCP8: Cap touch channel 8 positive terminal
18	14	PB3	AIO/DIO	PB3: GPIO TCN8: Cap touch channel 8 negative terminal
19	-	PB4	AIO/DIO	PB4: GPIO TCP9: Cap touch channel 9 positive terminal
20	-	PB5	AIO/DIO	PB5: GPIO

				TCN9: Cap touch channel 9 negative terminal
21	-	PB6	DIO	PB6: GPIO TCP10: Cap touch channel 10 positive terminal
22	-	PB7	DIO	PB7: GPIO TCN10: Cap touch channel 10 negative terminal
23	15	PB8	DIO	PB8: GPIO TCP11: Cap touch channel 11 positive terminal
24	16	PB9	DIO	PB9: GPIO TCN11: Cap touch channel 11 negative terminal PWM0_CHA: PWM0 output A GPT0_EXT_IN: GPT0 external input
25	17	PB10	DIO	PB10: GPIO TCP12: Cap touch channel 12 positive terminal PWM0_CHB: PWM0 output B
26	18	PB11	DIO	PB11: GPIO TCN12: Cap touch channel 12 negative terminal PWM1_CHA: PWM1 output A GPT1_EXT_IN: GPT1 external input
27	19	PB12	DIO	PB12: GPIO TCP13: Cap touch channel 13 positive terminal PWM1_CHB: PWM1 output B
28	20	PB13	DIO	PB13: GPIO TCN13: Cap touch channel 13 negative terminal PWM2_CHA: PWM2 output A GPT2_EXT_IN: GPT2 external input
29	-	PB14	DIO	PB14: GPIO PWM0_CHA: PWM0 output A
30	-	PB15	DIO	PB15: GPIO PWM0_CHB: PWM0 output B
31	-	PB16	DIO	PB16: GPIO PWM1_CHA: PWM1 output A GPT1_EXT_IN: GPT1 external input
32	-	PB17	DIO	PB17: GPIO PWM1_CHB: PWM channel 3

33	21	PB18	DIO	PB18: GPIO CSN: SPI chip select, active low
34	22	PB19	DIO	PB19: GPIO SCLK: SPI clock SCL: I2C clock SWCLK: SWD interface, clock signal
35	23	PB20	DIO	PB20: GPIO SIN: SPI data in SDA: I2C data SWDIO: SWD interface, data signal
36	24	PB21	DIO	PB21: GPIO SOUT: SPI data out
37	25	PB22	DIO	SWDIO: SWD interface, data signal PB22: GPIO PWM3_CHA: PWM3 output A GPT3_EXT_IN: GPT3 external input
38	26	PB23	DIO	SWCLK: SWD interface, clock signal PB23: GPIO PWM3_CHB: PWM3 output B
39	-	PB24	DIO	PB24: GPIO PWM2_CHA: PWM2 output A GPT2_EXT_IN: GPT2 external input
40	-	PB25	DIO	PB25: GPIO PWM3_CHA: PWM3 output A GPT3_EXT_IN: GPT3 external input
41	-	PB26	DIO	PB26: GPIO PWM3_CHB: PWM3 output B
42	-	PB27	DIO	PB27: GPIO PWM4_CHA: PWM4 output A GPT4_EXT_IN: GPT4 external input
44	28	PB28	DIO	PB28: GPIO PWM4_CHA: PWM4 output A GPT4_EXT_IN: GPT4 external intput PRINT_UART_TX: Print UART TX pin
45	29	PB29	DIO	PB29: GPIO PWM4_CHB: PWM4 output B UART_TX: UART transmission pin
46	30	PB30	DIO	PB30: GPIO PWM2_CHB: PWM2 output B UART_RX: UART receive pin

		E-PAD		Connected to GND inside package

P: Power supply pin DIO: Digital input and output pin AIO: Analog input and output pin

Note: The first function of the multiplexed pin is the default function after power-on reset.

6. Electrical Characteristics

Unless specified otherwise, all voltages are referenced to GND.

Unless specified otherwise, typical values stated where TA = 25℃ and VDD = 3.3V, Min/Max values stated where TA = -40℃ to 105℃ and VDD = 2.8V to 5.5V.

6.1. Absolute Maximum Ratings

Symbol	Description	Conditions	Min.	Max.	Unit
VDD	Power supply voltage		-0.3	5.8	V
I_{VDD}	Current into VDD pin	T = [-40, 105] ˚C	-	100	mA
I_{GND}	Current out of a GND pin	T = [-40, 105] ˚C	-	100	mA
V_{PIN}	Pin voltage with respect to GND		-0.3	VDD+0.3	V
I_{INJ_PAD}	Single IO pin input injection current		-10	10	mA
I_{INJ_SUM}	Sum of all input injected current		-50	50	mA

Note: Stresses beyond those listed in this section may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2. ESD Ratings

ESD Type	ESD Ratings
HBM	±8KV
CDM	±2KV
Latch-up	±100mA @ 105℃

6.3. Recommended Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
VDD (1)	Operating supply voltage	2.8		5.5	V
TA	Operating ambient temperature range	-40	-	105	℃
f_{CLK_CPU}	Nominal operating system clock frequency	0	-	32	MHz

1. If PGA is enabled, VDD should be > 2.97V.

6.4. Wake-Up Time

Symbol	Description	Min.	Typ.	Max.	Unit
$T_{wake-idle}$	Wake-up time from IDLE mode（1） Waking up the CPU needs is 5 clock cycles. Interrupt response time is 16 clock cycles	-	21 clock cycles	-	-
$T_{wake-sleepwalk}$	Wake-up time from SLEEPWALK mode（1） (CPU is clocked by RC16M with the frequency of 16MHz)	-	21	-	μs
$T_{wake-sleep}$	Wake-up time from SLEEP Mode（1） (CPU is clocked by RC16M with the frequency of 16MHz)	-	320	-	μs

1. The time is from the occurrence of an interrupt and until entering the interrupt handler. Based on characterization result.

6.5. Power Consumption

Parameter Name	Parameter	Min.	Typ.（1）	Max.	Unit	Condition
Active power consumption	I_{DD_ACTIVE}	-	2.3	-	mA	CPU frequency of 16MHz, Watchdog is enabled
Sleepwalk power consumption	$I_{DD\_Sleepwalk}$	-	1.1	-	mA	Base current. All peripherals that can be disabled are disabled.
Sleep power consumption (1)	I_{DD_SLEEP}	-	3.8	45	uA	Base current. All peripherals that can be disabled are disabled.

1. Based on characterization result

6.6. POR Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
V_{POR}(1)	POR voltage (VDD rising)	1.69	2	2.34	V
Tr_pwrup	Power up time	1	-	-	us
T_{POR}	To ensure successful power on again, VDD needs to be kept below V_{POR} for T_{POR} at least.	-	10	-	us
I_{POR}(1)	Power consumption	-	0.1	-	uA

1. Guaranteed by design, not tested in production

6.7. RC16M Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Power consumption(1)		-	315	-	uA

Frequency		-	16	-	MHz
Frequency error	After trimmed	-3		3	%
Frequency temperature drift (2)			125		PPM/°C
Duty cycle		40		60	%

1. Based on characterization result
2. Guaranteed by design, not tested in production

6.8. RC32K Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Power consumption(1)		-	0.3	-	uA
Frequency		-	32.768	-	KHz
Frequency error		-19		19	%
Frequency temperature drift (1)			125		PPM/°C
Duty cycle		40		60	%

1. Guaranteed by design, not tested in production

6.9. Frequency Doubler Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Power consumption（1）		-	40	-	uA
Input frequency range		-	16	-	MHz
Frequency multiplication		-	2	-	

1. Guaranteed by design, not tested in production

6.10. GPIO Characteristics

Symbol	Conditions	Min.	Typ.	Max.	Unit
VIL	VDD=5V	-	-	0.3VDD	V
	VDD=3.3V	-	-	0.8	V
VIH	VDD=5V	0.7VDD	-	-	V
	VDD=3.3V	2.0	-	-	V
VHYS	Schmitt trigger hysteresis PINMUX.Pxx_CFG.CS = 0	0.1VDD	-	-	V
VOH	VDD=5V, driving current 10mA	VDD-0.8	-	-	V
	VDD=3.3V, driving current 5mA	2.4			V
VOL	VDD=5V, driving current 10mA	-	-	0.5	V
	VDD=3.3V, driving current 5mA	-	-	0.3	V
Rpup	IO	-	90	150	KΩ

CIN	IO input capacitance	-	-	10	pF
Tr/Tf Rising time or falling time	VDD=5V, low driving strength (DR=1), slow slew rate(SR=1) Cloading = 50pF	-	-	10.36	nS
	VDD=5V, high driving strength (DR=0), fast slew rate(SR=0) Cloading = 50pF	-	-	5.13	nS
	VDD=3.3V, low driving strength (DR=1), slow slew rate(SR=1) Cloading = 50pF	-	-	16.38	nS
	VDD=3.3V, high driving strength (DR=0), fast slew rate(SR=0) Cloading = 50pF	-	-	8.19	nS

6.11. PGA Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
VDD range for PGA	PGA working	2.97		5.5	V
Power consumption（1）		500		1000	uA
Power consumption when disable（2）		-	10	-	nA
Start-up time if enabled（2）			10		us
Input common voltage range		0.2		VDD-1.4	V
Input differential voltage range	Vref: ADC Vref	-0.9Vref/Gain		0.9Vref/Gain	V
Gain（PGA1）	1X,2X,4X,8X,16X,32X	-	1/2/4/8/16/32X	-	
Gain（PGA1）	1X,2X,4X,8X,16X,32X	-	1/2/4/8/16/32X	-	
Gain accuracy（2）		-	1	-	%
Gain drift versus temperature（2）	–40~85 ℃	-	±10	-	ppm/℃
Programmable levels for power consumption		-	0.6/0.8/1/1.2X	-	
Offset	Offset canceling not enabled	-	±5	-	mV
Offset Temperature Drift (2)	Offset canceling not enabled	-	±1	-	uV/℃
Quiescent current of IDAC1 and IDAC2		-	155	-	uA
IDAC1	control bits [5:0], Step current = 10uA	-	0/10/…/630	-	uA
IDAC2	Control bit [5:0], step	-	0/0.625/…/39.375	-	uA

	current = 0.625uA				
	Control bit [11:6], step current = 10uA	-	0/10/…/630	-	uA

1. Based on characterization result
2. Guaranteed by design, not tested in production

6.12. ADC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
Resolution	ADC resolution（with sign bit）	-	14	-	Bits
Power consumption（1）	VDD=3.3V	-	2.4	-	mA
Power consumption（1）	VDD=3.3V，ADC in low power mode	-	280	-	uA
Power consumption when disabled（1）		-	10	-	nA
Voltage reference	Vref	-	VDD, LDO VS internal 2.5V or 1.5V	-	
F_{ADC}	ADC clock frequency	0.025	-	16	MHz
Total conversion time (including sampling time)	PGA is bypassed, F_{ADC}=16MHz	1.6	-	-	us
	PGA1 or PGA2 or Both is used	12	-	-	us
ADC sampling clock cycles	PGA is bypassed, F_{ADC} = 25KHz ~ 16MHz	4			cycles
ADC conversion clock cycles	PGA is bypassed, F_{ADC} = 25KHz ~ 16MHz	21			cycles
V_{IN}	Differential input voltage range	-Vref	-	Vref	V
V_{CM}	ADC input common voltage range	0		Vref	V
Csample（1）		-	3.5		pF
Output resistance of external signals Rext	PGA is bypassed	-	-	10K	Ω
	PGA1 or PGA2 or Both is used	-	-	1M	
INL	F_{ADC}=16MHz, Rext ≤ 10KΩ	-4	±2	4	LSB
DNL	F_{ADC}=16MHz, Rext ≤ 10KΩ	-4	±2	4	LSB

1. Guaranteed by design, not tested in production

6.13. TinyTouch Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Capacitance of touch pad	Cx	-	10	-	pF	
Power consumption when disabled（1）		-	65	-	nA	
Average power consumption		-	65	-	uA	1 channel enabled, 10nF shared Cref, 16Hz detection frequency
		-	78	-	uA	2 channels enabled, 10nF shared Cref, 16Hz detection frequency
Internal analog switch Ron resistance	R_{AI_AO}	0.68	1	1.4	KΩ	VDD=3.3V, resistance of AI to AO
		0.67	0.9	1.2		VDD=5.5V, resistance of AI to AO
	R_{AI_GND}	0.68	1	1.5		VDD=3.3V, resistance of AI to GND
		0.67	0.9	1.25		VDD=5.5V, resistance of AI to GND

1. Guaranteed by design, not tested in production

6.14. LDO VS Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Noise(2)	e_{OUT}	-	5	10	uV_{RMS}	C_{VS}= 22nF, Freq in 1-20KHz
PSRR(1)	PSRR	34	40	48	dB	@10K Hz
		54	60	67	dB	@1Hz, at regulation mode
VS Voltage	Vvs	-	1.8	-	V	VDD ≥2.8V
		-	2.0	-	V	VDD ≥2.8V
		-	2.2	-	V	VDD ≥2.8V
		-	2.4	-	V	VDD ≥2.8V
		-	2.6	-	V	VDD ≥2.9V
		-	2.8	-	V	VDD ≥3.1V
		-	3.0	-	V	VDD ≥3.3V
		-	3.1	-	V	VDD ≥3.4V
Voltage accuracy (2)		-	±1	-	%	
Temperature drift (1)	T_{VS}	-	100	-	ppm/°C	

Dropout voltage		-	170	300	mV	
External capacitor on VS PIN	C_{VS}	-	22	-	nF	
	ESR	0.2	0.3	0.7	Ω	
The max. output current	I_{VSOUT}	15	-	-	mA	
Peak current at startup(1)	I_{VSPK}	-	-	120	mA	Peak current duration time ≤ 5us
		-	-	350	mA	Peak current duration time ≤ 0.5us
Short current	I_{VSSC}	23	30	80	mA	10Ω resistor to ground.
Quiescent current (1)	I_{VS}	230	250	400	uA	
Line regulation			3.2	9	mA	I_{VSOUT}=15mA, VDD from 2.8V to 5.5V
Load regulation		-	0.1	6.4	mA	I_{VSOUT} from 0.1mA to 15mA
Start-up time	$t_{startup}$	-	-	220	us	When power on @ 10us
		-	-	3	us	When LDO VS is enabled
VS Dividing Voltage	V_{VS_DIV}	0.27	0.3	0.33	V	CTRL_LDO3VS_DIV_SEL[2:0] = 000
		0.36	0.4	0.44	V	CTRL_LDO3VS_DIV_SEL[2:0] = 001
		0.45	0.5	0.55	V	CTRL_LDO3VS_DIV_SEL[2:0] = 010
		0.54	0.6	0.66	V	CTRL_LDO3VS_DIV_SEL[2:0] = 011
		0.63	0.7	0.77	V	CTRL_LDO3VS_DIV_SEL[2:0] = 100
		0.72	0.8	0.88	V	CTRL_LDO3VS_DIV_SEL[2:0] = 101
		0.81	0.9	0.99	V	CTRL_LDO3VS_DIV_SEL[2:0] = 110
		0.9	1.0	1.1	V	CTRL_LDO3VS_DIV_SEL[2:0] = 111

1. Guaranteed by design, not tested in production
2. Based on characterization result

6.15. LVD Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Power consumption when enabled（1）	I_{LVD}	-	11		uA	LVD enabled
Power consumption when disabled（1）		-	1	-	nA	LVD disabled

Voltage threshold	V_{LVD}	2.82	2.88	2.94	V	LVD Level0, falling
		2.93	2.99	3.05	V	LVD Level0, rising
		3.05	3.11	3.17	V	LVD Level1, falling
		3.15	3.21	3.27	V	LVD Level1, rising
		1.60	3.71	3.82	V	LVD Level2, falling
		3.80	3.91	4.02	V	LVD Level2, rising
		4.37	4.48	4.59	V	LVD Level3, falling
		4.58	4.69	4.80	V	LVD Level3, rising

1. Guaranteed by design, not tested in production

6.16. Flash Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Data retention		10	-	-	Years	
Flash programming write cycles		20000	-	-	Cycles	
Word programming time	$t_{PROGWORD}$	-	-	6.5	us	
Page-erase time	$t_{PAGEERASE}$	-	-	3	ms	
Flash-read current	$I_{FLASHREAD}$	-	1.25	3.5	mA	CPU clock frequency 16MHz
Flash-write current	$I_{FLASHWRITE}$	-	-	3.5	mA	
Flash-erase current	$I_{FLASHERASE}$			2	mA	

7. Detailed Description

7.1. Processor

The device integrates 32-bit Arm® Cortex®-M0 CPU core with the maximum operating clock frequency of 32MHz.

7.2. Memory

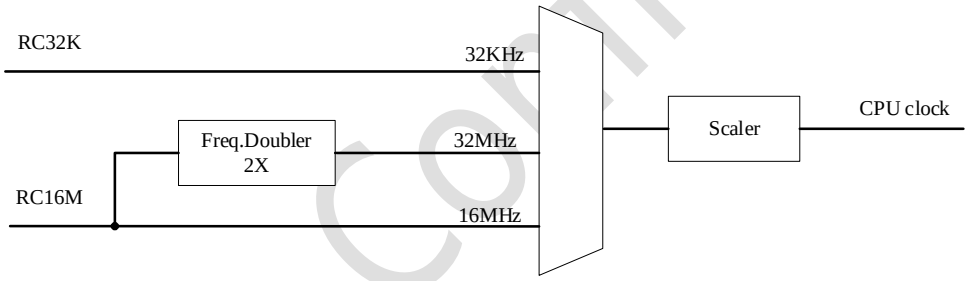
The device has 64KB Flash and 8KB SRAM.

7.3. Clock system

The clock system includes the following clock sources:

- Internal high-speed clock RC16M
- Internal low-speed clock RC32K

RC16M generates a 16MHz clock, which can be multiplied to 32MHz by a frequency doubler. The clock source for CPU can be RC16M output (16MHz), frequency doubler output (32MHz), or the low-speed clock (RC32K).



7.4. RESET

The chip supports 4 reset sources:

- POR power-on reset
- LVD low voltage detection reset
- WDG watchdog reset
- Software reset

7.5. Interrupt System

The Cortex®-M0 processor has a built-in NVIC interrupt controller, which supports up to 32 interrupt vectors. The interrupt sources and interrupt vector configuration in this chip are shown in the table below. The user program runs from the Flash start address 0x1000_0000. The formula calculating an interrupt's entry address is: 0x1000_0040 + interrupt vector number*4.

Interrupt vector number	Interrupt source	Description
0	FLASH_ERROR	Flash error
1	FLASH_PROG	Flash programming is completed
2	FLASH_ERASE	Flash erase complete
3	I2C_IRQ	I2C data sending and receiving interrupt
4	UART_IRQ	UART interrupt
5	GPT0_IRQ	General Purpose Timer0 interrupt
6	GPT1_IRQ	General Purpose Timer1 interrupt
7	GPT2_IRQ	General Purpose Timer2 interrupt
8	GPT3_IRQ	General Purpose Timer3 interrupt
9	GPT4_IRQ	General Purpose Timer4 interrupt
10	WDG_IRQ	Watchdog timeout interrupt
11	TINYTOUCH_IRQ	TinyTouch interrupt
12	DMA_IRQ	DMA interrupt
13	ADC_CMP	ADC compare interrupt
14	ADC_DONE	ADC trigger done
15	ADC_FIFOFULL	ADC FIFO full
16	ADC_FIFORDY	ADC FIFO ready when DMA/TRIG not enabled
17	ADC_FIFOEPT	ADC FIFO empty
18	GPIOA_IRQ	GPIOA interrupt
19	RTC_IRQ	RTC timeout
20	LVD_IRQ	VDD low voltage
21	LVD15_IRQ	LDO15 low voltage
22	SPI_IRQ	SPI interrupt
23	GPIOB_IRQ	GPIOB interrupt
24-31	Not used	

7.6. Working Mode

The device supports 4 working modes: active mode (ACTIVE), idle mode (IDLE), sleep walk mode (SLEEPWALK) and sleep mode (SLEEP).

- Active mode (ACTIVE): The CPU core runs at full speed according to the CPU clock setting. And all enabled peripherals run.
- Idle mode (IDLE): The CPU core clock is stopped. All the enabled peripherals are allowed to continue operating. The CPU core has no task running and is in the WFI (Wait For Interrupt) state. Any interrupt can wake up the system and restart the CPU core clock. The system wakes up from this mode with the shortest wake-up time.
- Sleep Walk Mode (SLEEPWALK): Part of peripherals can be enabled on demand. And some of them can work under Tinywork® mechanism. The power consumption in this mode is between idle mode and sleep mode, depending on which peripherals are working.
- Sleep mode (SLEEP): RC16M clock is disabled, peripherals that need RC16M are not allowed to run. The 32K clock continues operating.

Module	Module Sates in different working modes			
	ACTIVE	IDLE	SLEEPWALK	SLEEP
CPU CORE	ON	WFI	WFI	WFI
FLASH	ON	ON	OFF	OFF
SRAM	ON	ON	ON	OFF
DMA	ON/OFF	ON/OFF	ON/OFF	OFF
GPIO	ON/OFF	ON/OFF	ON/OFF	ON/OFF
UART	ON/OFF	ON/OFF	ON/OFF	OFF
Print UART	ON/OFF	ON/OFF	ON/OFF	OFF
I2C	ON/OFF	ON/OFF	OFF	OFF
SPI	ON/OFF	ON/OFF	OFF	OFF
GPT0-4	ON/OFF	ON/OFF	OFF	OFF
WDG	ON/OFF	ON/OFF	ON/OFF	ON/OFF
RTC	ON/OFF	ON/OFF	ON/OFF	ON/OFF
Debug	ON	ON	OFF	OFF
Tinywork®	ON/OFF	ON/OFF	ON/OFF	OFF
TinyTouch	ON/OFF	ON/OFF	ON/OFF	OFF
POR	ON	ON	ON	ON
LVD	ON/OFF	ON/OFF	ON/OFF	OFF
ADC	ON/OFF	ON/OFF	ON/OFF	OFF
PGA	ON/OFF	ON/OFF	ON/OFF	OFF
RC16M	ON/OFF	ON/OFF	ON/OFF	OFF
RC32K	ON	ON	ON	ON
LDO15	ON	ON	ON	Low power operating
LDOVS	ON/OFF	ON/OFF	ON/OFF	OFF

Note:

ON: The module is running

OFF: The module can not be enabled and stays in a non-working state

ON/OFF: If the module is enabled, it is running; but if not enabled, it is in non-working state

WFI: The CPU is in a low power consumption state and can be awakened by interrupts.

7.7. General Purpose Input/Output - GPIO

GPIO can be configured as internal pull-up/pull-down input, high-impedance input, push-pull output, and open-drain output. When configured as an input, Schmitt input feature can be enabled to add hysteresis between the input High/Low thresholds.

GPIO can be used as an external interrupt, supporting edge triggering and level triggering, and can wake up the device from IDLE/SLEEPWALK/SLEEP mode to the ACTIVE mode.

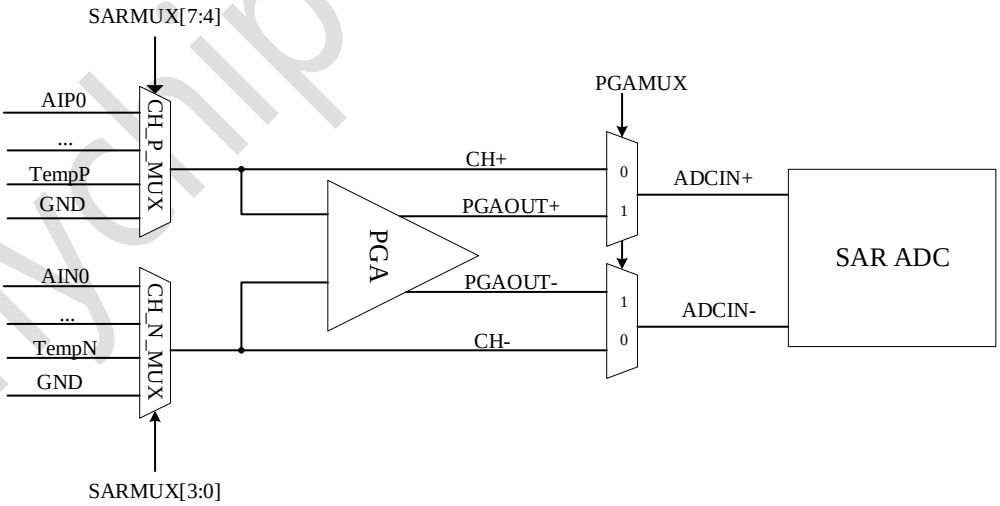
Refer to pin function table for the multiplexing between GPIO and other functions.

7.8. Analog-to-Digital Converter - ADC

The ADC module can transform external or internal analog signals on selected ADC inputs into a digital representation. It is connected to an analog input multiplexer for selection between multiple single-ended and differential inputs. This module is a 14-bit Successive Approximate Register (SAR) ADC, with PGA, offset cancellation, reference voltage generation, conversion result comparison etc.

The ADC supports 8 external differential channels from VIP0/VIN0 to VIP7/VIN7, or 16 external single-ended channels by VIP0-VIP7 and VIN0-VIN7 pins, as well as 1 internal differential channel for on-chip temperature sensor.

A channel can be routed to SAR ADC directly or through PGA for sampling and conversion. The channel MUX is shown in the figure below.



The ADC voltage reference can be on-chip LDOVS output, or on-chip ADC_VREF. ADC_VREF is generated by the ADC module and can be configured as 1.5V or 2.5V to provide a reference voltage for the ADC.

The ADC has two-stage PGA, PGA1 and PGA2, which amplifies input differential signal. Each level has configurable gains of 1/2/4/8/16/32X, so two levels of PGA can amplify the signal up to 1024 times.

ADC has differential offset voltage cancellation circuit, which works with PGA1. With proper parameter

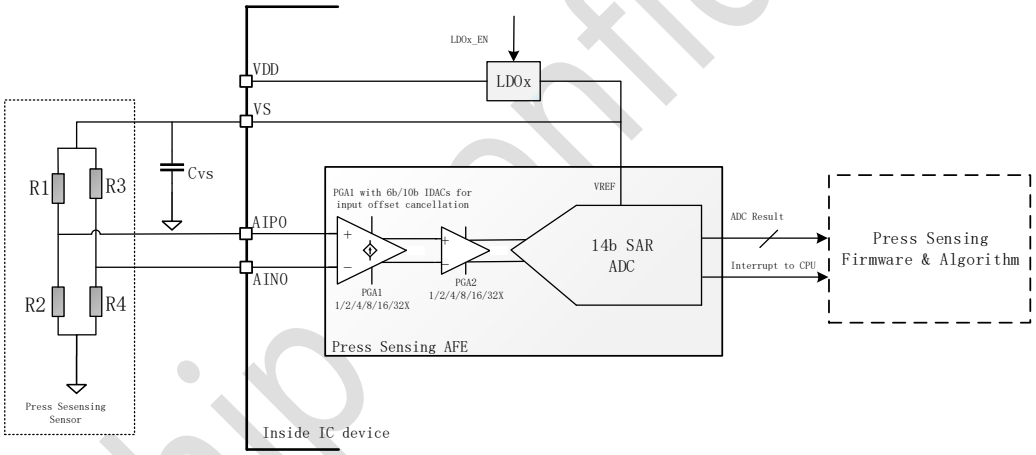
settings, the offset cancellation circuit can generate approximately the same amount of voltage which is opposite to the input differential offset, so offset voltage is almost removed before the signal enters ADC. In this way, desired weak signal is kept and amplified while the input offset is eliminated.

The ADC conversion result can be compared with two preset thresholds, CMPTHH and CMPTHL. If the following conditions are met, an interrupt (if enabled) is generated.

- Between the two thresholds, CMPTHH and CMPTHL
- Not lower than the upper threshold CMPTHH
- Not higher than the lower threshold CMPTHL

ADC conversion can be triggered by software. It can also be triggered by other peripherals through the Tinywork® mechanism, for example, the RTC can be used to trigger ADC to start conversion at regular intervals (RTC timeout). After the ADC is started, the selected several channels are converted sequentially. When the conversion on selected channels is complete, an interrupt can be triggered. The ADC conversion result is stored in the register or FIFO, and DMA can also be used to automatically transfer the result data to the specified SRAM address.

The following figure is the block diagram demonstrating pressure detection using ADC on a force sensor of Wheatstone bridge.

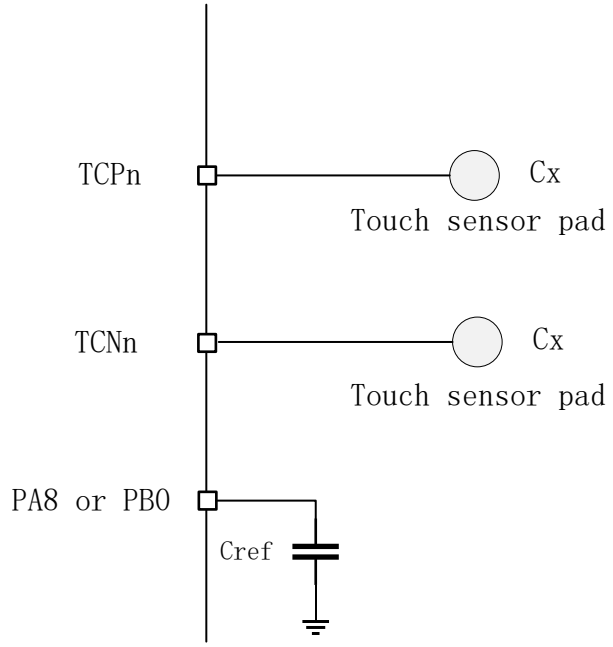


7.9. Capacitive Touch Controller- TinyTouch

The capacitive touch controller (TinyTouch) can be used to monitor the relative change on the capacitance of the external capacitive sensor to detect user's touch operations. With the dedicated touch algorithm, it can detect touching gestures on touch buttons (single or double click) and sliders etc.

TCAE32 TinyTouch module works with self-capacitance sensors, and supports two touch blocks, Touch Block0 and Touch Block1. Each touch block supports 13 channels with shared reference capacitance (Cref).

All channels of a touch block share a reference capacitor Cref, which is connected to a dedicated pin, PA8 for Touch Block0, and PB0 for Touch Block1. The shared Cref can be used if the touch sensor and parasitic capacitance are similar on all channels in a touch block.



ADC is used to measure directly the Cref voltage and then firmware determines the capacitance variance.

7.10. Internal Temperature Sensor - Tsensor

The output voltage of the internal temperature sensor has a linear relationship with the on-chip temperature. It is a differential analog voltage, which is connected to the ADC input terminals for conversion. After computation based on ADC result, the on-chip temperature can be determined.

7.11. Watchdog - WDG

The watchdog (WDG) of this chip uses the internal RC32K clock, and the timeout time is configurable from 0.1ms to 32s. It can be configured to generate an interrupt or directly reset the chip when the watchdog timeout occurs.

7.12. Low Voltage Detector - LVD/LVD15

LVD and LVD15 monitor the VDD voltage or the internal 1.5V voltage respectively. When the detected voltage is lower than the preset threshold, it can reset the chip, if it is configured to reset mode.

Or it can be configured to interrupt mode, under which LVD/LVD15 will generate an interrupt if the following conditions are met:

- Below the threshold
- Cross the threshold during the voltage rising process
- Cross the threshold during the voltage falling process

LVD/LVD15 supports configured filters of multiple levels to prevent false triggers.

7.13. Inter-Integrated Circuit Bus - I2C

The I2C module supports four working modes: host sending, host receiving, slave sending, and slave receiving. It supports two speed rates, standard 100KHz and fast 400KHz. It has 8-byte receive (RX) FIFO and 8-byte

transmit (TX) FIFO. And DMA can be used with I2C to convey received data or data to send.

The I2C pins (SDA/SCL) are open-drain outputs, which support typical external pull-up voltages, 3.3V or 5V.

7.14. Universal asynchronous serial interface - UART/Print UART

This chip includes two UART controllers UART and Print UART.

UART module is a full-duplex communication interface for both sending and receiving data simultaneously. This module can also support LIN Slave and can work with DMA for data convey.

Print UART is a send-only interface, which is normally used to output debugging information or log information.

7.15. SPI

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows full duplex communication between TCAE32 device and peripheral devices, or between several microcontrollers. The SPI module can be configured as either master or slave. The master initiates and controls all data transactions.

7.16. GPT0-4

The device integrates five General Purpose Timer GPT0-4. A GPT consists of a base counter and a set of compare/match logics. The base counter can be used to count internal clock cycles or external pulse input. The counter has direction and period settings, and can be configured as “saw tooth wave” counting (counting upwards from zero, and return zero when reaching the max value), or “tri-angle wave” counting (counting upwards firstly and then backwards). Multiple levels of compare/match logics can be used with the base counter for pulse generation, or PWM modulation. A GPT has two output pins, which can output a pair of complementary signals or two independent signals.

7.17. Direct memory access - DMA

The DMA controller can support up to 3 channels of DMA transmission at the same time. The channel can be configured for data transfer between one of the peripherals listed below and a specified SRAM address space.

DMA peripheral number *	DMA peripheral request	Data transmission direction
3	I2C TX	Peripheral <- memory
4	I2C RX	Peripheral - > memory
5	UART TX	Peripheral <- memory
6	UART RX	Peripheral - > memory
7	SPI TX	Peripheral <- memory
8	SPI RX	Peripheral - > memory
9	TinyTouch	Peripheral - > memory

10	ADC	Peripheral - > memory

*Note: The DMA peripheral number is the same as the channel MAP request register DRCMRx number, i.e., DRCMR3 corresponds to the I2C TX peripheral request.

7.18. Real time clock controller - RTC

RTC has a 16-bit timer/counter using RC32K clock (or scaled) as its clock source. Four different counting thresholds are supported by RTC. Every time a threshold is reached, an interrupt is generated. The RTC timeout can also be used to trigger other peripherals to start running thanks to the Tinywork® mechanism.

7.19. Programming and debugging interface - SWD

Support two-wire serial programming and debugging interface SWD and support JLINK and CMSIS-DAP tools for debugging and development.

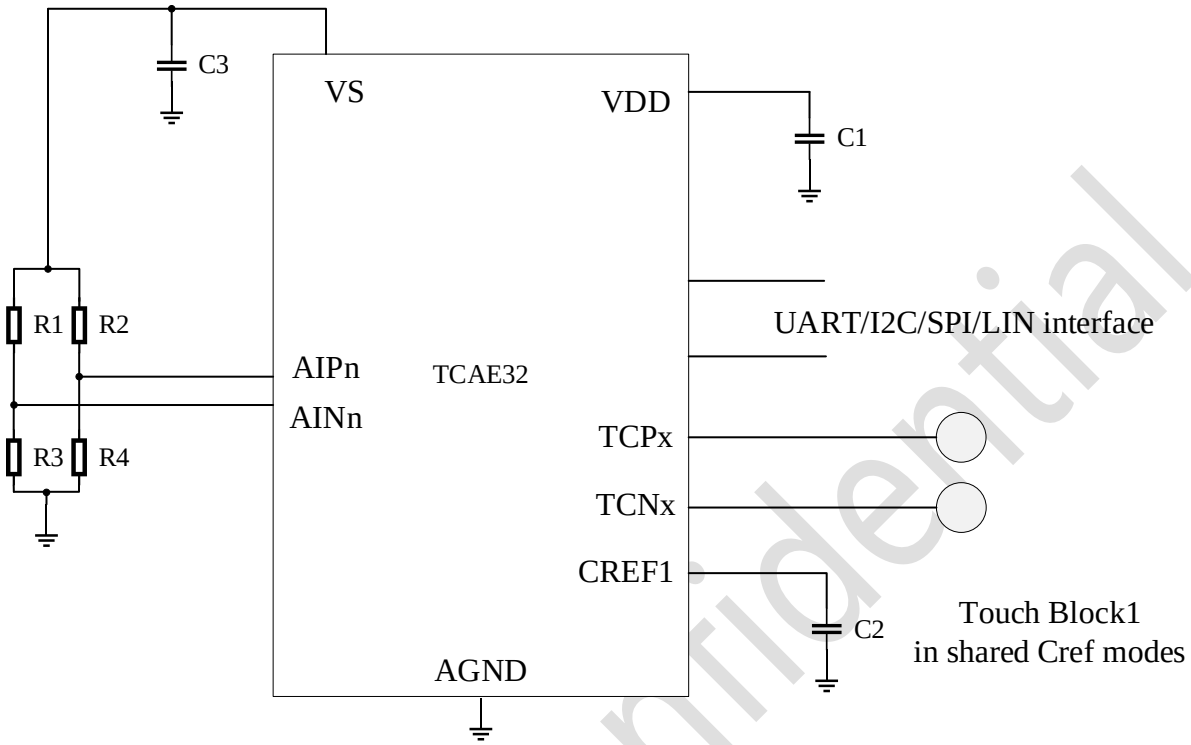
7.20. Tinywork®

Tinywork® is a special mechanism deployed in Tinychip MCUs to reduce power consumption. It realizes event signal transmission between peripherals under low power modes. By this way, different modules are linked and can be triggered to start working without CPU participation. And in low power modes, if needed, Tinywork® can even shift the MCU's working mode before transmit a triggering signal. Its main benefits include faster response, more flexible configuration and lower power consumption.

7.21. UUID

96-bit UUID is provided on-chip. The UUID information is written at factory, and the content cannot be changed by customers.

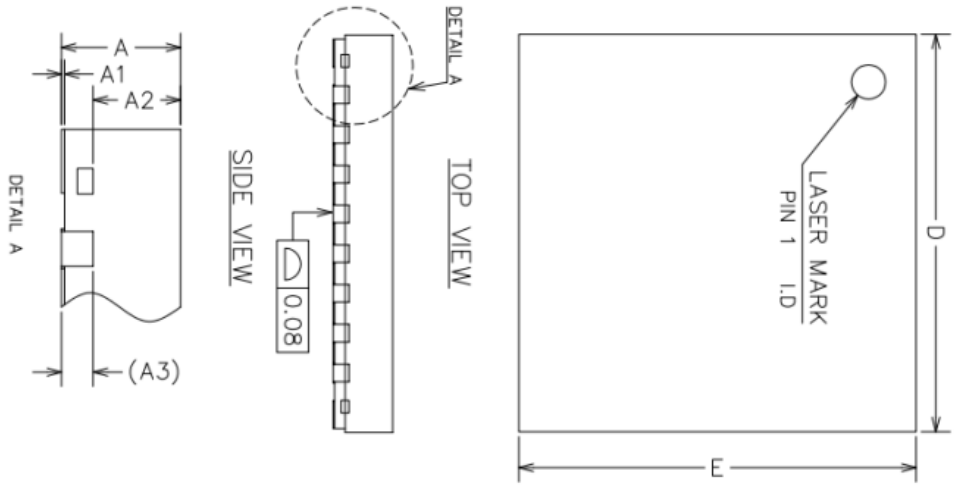
8. Application Circuit Example

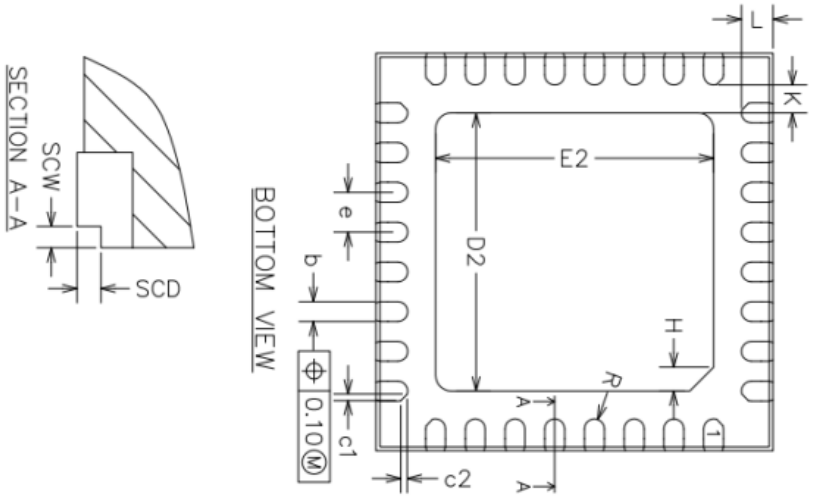


9. Package and Carrier Information

9.1. Package Drawing

9.1.1. QFN32

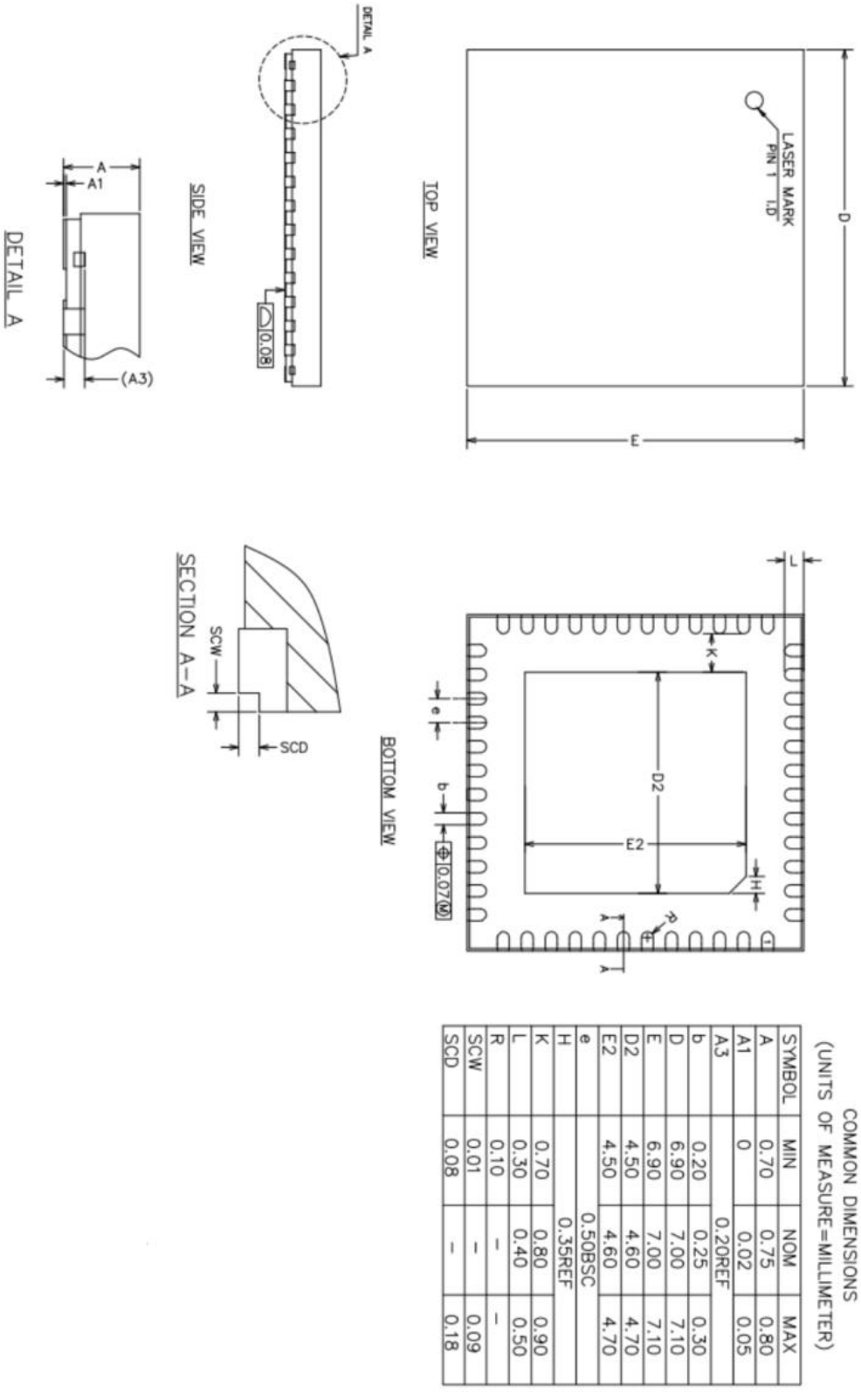




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60
e	0.40	0.50	0.60
H		0.30REF	
K		0.35REF	
L	0.30	0.40	0.50
R	0.09	–	–
c1	–	0.08	–
c2	–	0.08	–
SCW	0.01	–	0.09
SCD	0.08	–	0.18

9.1.2. QFN48



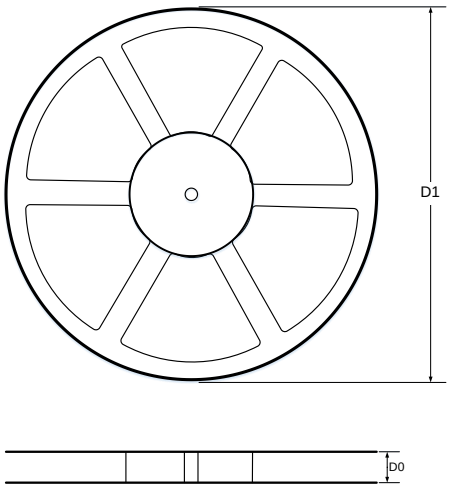
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
e		0.50BSC	
H		0.35REF	
K	0.70	0.80	0.90
L	0.30	0.40	0.50
R	0.10	–	–
SCW	0.01	–	0.09
SCD	0.08	–	0.18

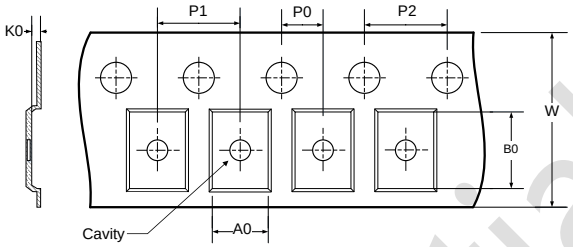
9.2. Carrier Materials Information

9.2.1. QFN32

REEL DIMENSIONS

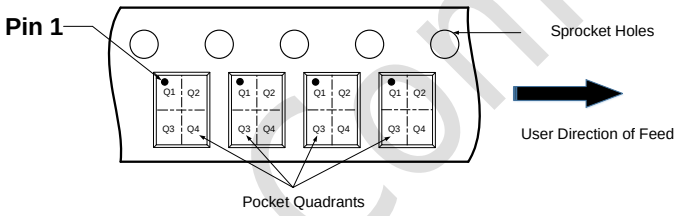


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



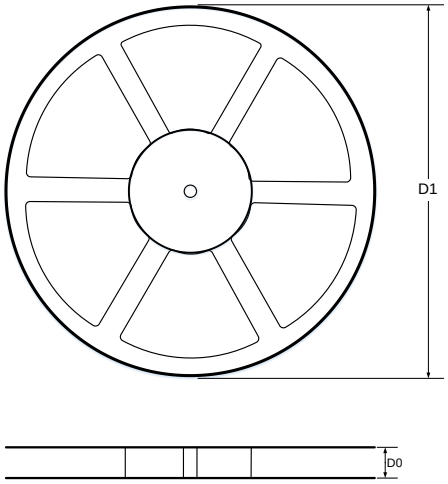
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	12.40	5.30	5.30	1.10	2.00	8.00	4.00	12.00	Q1

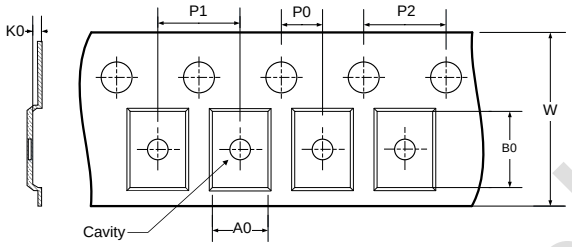
All dimensions are nominal

9.2.2. QFN48

REEL DIMENSIONS

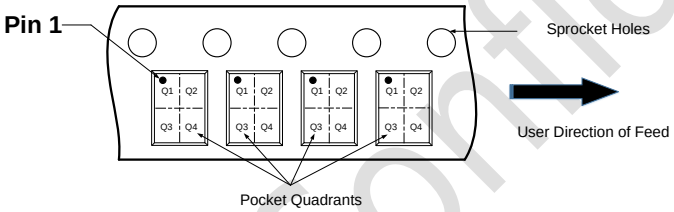


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330.00	16.40	7.30	7.30	1.20	2.00	12.00	4.00	16.00	Q1

All dimensions are nominal

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Revision

Revisions	Date	Comments
1.0	2023/9/1	v1.0 release

About Us

Tinychip Microelectronics Co., Ltd. was established in Zhangjiang, Shanghai in 2019. As a leading supplier of high-performance dedicated SoC IC in China, the company focuses on the research and development of various chips related to Internet of Things applications, and has received firm and powerful support as well as investments from selected top investment institutions. The company is joined with a group of top semiconductor experts and is committed to developing into a platform company in semiconductor industry. The team has the research and development capabilities of various system-level complex IC products, and the total shipments have reached billions of units. The company has developed a large number of SoC IC based solutions in analog signal chain, power supply and radio frequency, which cover consumer electronics, industrial control and automotive applications. While setting the industry's new benchmarks with differentiated IC products, they will empower more IoT companies and better serve customer needs.

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